

# Avnet Embedded Vision Multi-Sensor FMC

## Hardware User Guide

Version 1.04

September 2021

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**Document Version:**           **Version 1.04**

**Document Date:**            29 September 2021

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<b>Prior Version History:</b>	Version:	Date:	Comment:
	1.01	10/15/2018	Avnet Multi-Camera FMC Module (GMSL only version)
	1.02	09/21/2021	Removed all references to GMSL2 and "Phase 2" solution which is no longer planned for this Avnet solution to avoid confusion. Also, removed 3D renderings of FMC and replaced with actual product photos.
	1.03	09/21/2021	Adjusted document title from "MicroZed" to more accurately reflect contents.
	1.04	09/29/2021	Cleaned up broken links and references.

**Comments:**

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# 1. Introduction

The purpose of this manual is to describe the functionality and contents of the Avnet Embedded Vision Multi Sensor FMC Module. This document includes descriptions of the hardware features.

## 1.1 Description

The Avnet Embedded Vision Multi Sensor FMC Module is not a stand-alone module, but rather a plug-in module designed to interface with FMC compatible baseboards. In that role, the FMC adapter supports multiple cameras for Xilinx Zynq UltraScale+ embedded vision applications in automotive ADAS, augmented reality and UAV / drones.

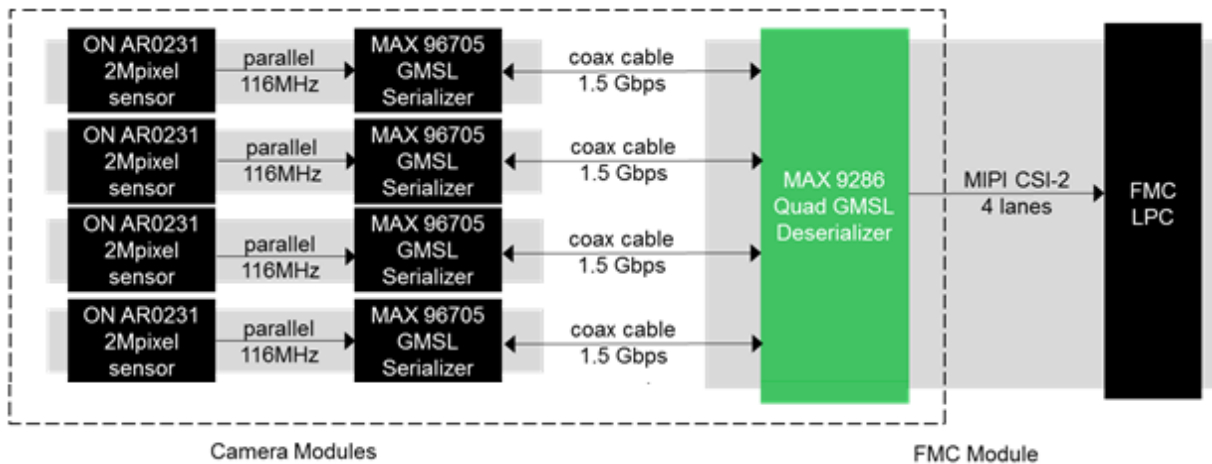


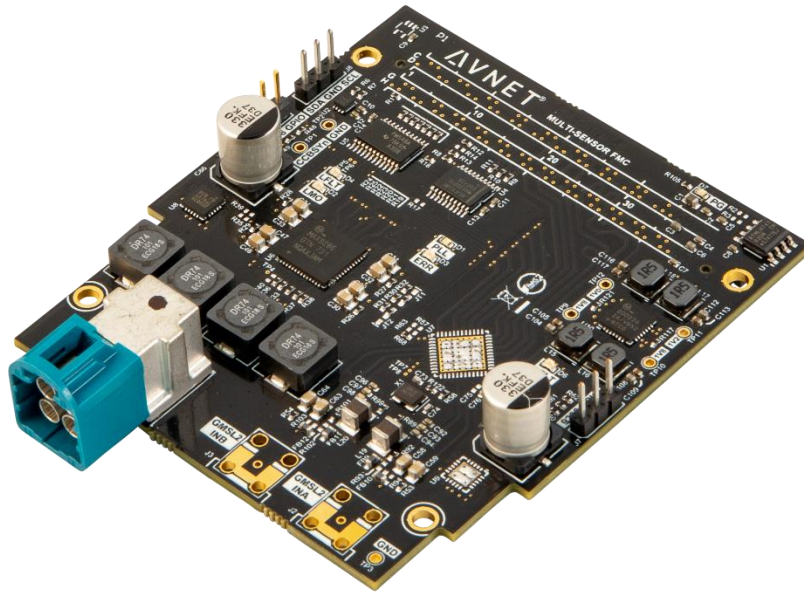
Figure 1 - Avnet Embedded Vision Multi Sensor FMC – System Diagram

As shown in the system diagram above, the FMC Module supports a total of 4 2Mpixel Camera Modules connected remotely over 50Ω Coax (100Ω STP) Cables.

## 1.2 Ordering Information

The Multi-Camera FMC module supports only GMSL and there are no plans to support GMSL2 with this hardware.

Supplier	Part Number	Description	Resale
Avnet	AES-FMC-MULTICAM4-G	Multi-Camera FMC Module (Quad GMSL only)	\$299

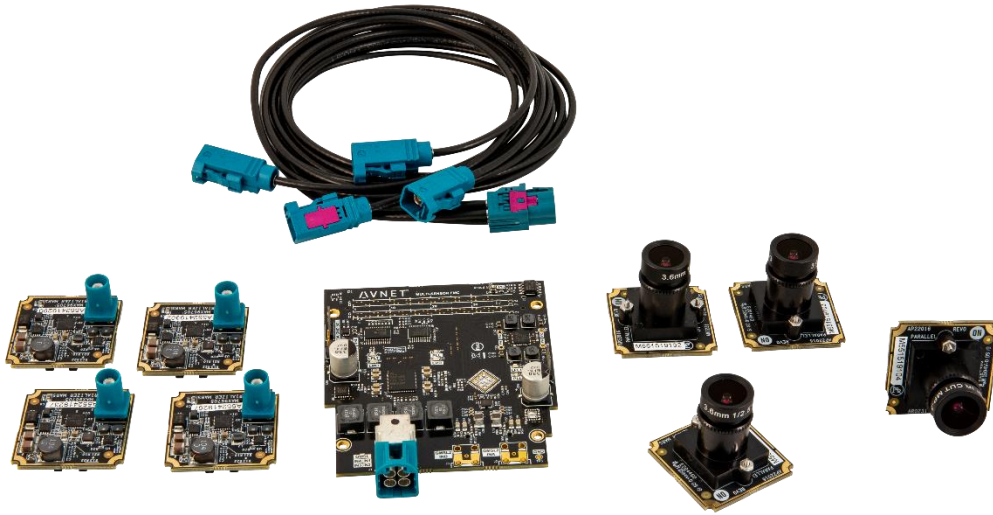


The following table lists the components required to create a complete Quad Camera FMC solution.

Supplier	Part Number	Description	Resale
Avnet	AES-FMC-MULTICAM4-G	Multi-Camera FMC Module (Quad GMSL only)	\$299
Rosenberger	L02-027-1000-Z-ZZZZ_V2	Quad HFM to 4 FAKRA Cable Assembly	\$69
ON Semiconductor	MARS1-MAX96705-GEVK	MAX96705 Serializer Kit	4 x \$250
ON Semiconductor	MARS1-AR0231AT7-GEVB	AR0231AT Image Sensor Board	4 x \$250
<b>TOTAL</b>			<b>\$2468</b>

Avnet is providing the following bundle, with 30% discount over individual pricing.

Supplier	Part Number	Description	Resale
Avnet	AES-FMC-MC4-AR0231AT-G	Quad Camera FMC Bundle	\$1699



## 1.3 References

ON Semiconductor MARS – Modular Automotive Reference System:

<https://www.onsemi.com/solutions-applications/segments/automotive/adas-viewing-autonomous-vehicles/mars-modular-automotive-reference-system>

ON Semiconductor AR0231AT:

<https://www.onsemi.com/products/sensors/image-sensors/ar0231at>

Xilinx MIPI D-PHY v3.1 (PG202):

[https://www.xilinx.com/support/documentation/ip\\_documentation/mipi\\_dphy/v3\\_1/pg202-mipi-dphy.pdf](https://www.xilinx.com/support/documentation/ip_documentation/mipi_dphy/v3_1/pg202-mipi-dphy.pdf)

Xilinx MIPI CSI-2 RX Sub-system v2.2 (PG232):

[https://www.xilinx.com/support/documentation/ip\\_documentation/mipi\\_csi2\\_rx\\_subsystem/v2\\_2/pg232-mipi-csi2-rx.pdf](https://www.xilinx.com/support/documentation/ip_documentation/mipi_csi2_rx_subsystem/v2_2/pg232-mipi-csi2-rx.pdf)

Xilinx package pinout References:

UZEV CC – <https://www.xilinx.com/support/packagefiles/zuppackages/xczu7evfbvb900pkg.txt>

ZCU102 – <https://www.xilinx.com/support/packagefiles/zuppackages/xczu9egffvb1156pkg.txt>

ZCU104 – <https://www.xilinx.com/support/packagefiles/zuppackages/xczu7evffvc1156pkg.txt>

## 2. Block Diagram and Features

This section summarizes the features of the Avnet Embedded Vision Multi-Sensor FMC module, followed by functional descriptions.

### 2.1 Features

The Avnet Embedded Vision Multi Sensor FMC Module provides the following features:

- FMC LPC (Low Pin Count)
- Quad 2Mpixel Camera Module support, via
  - Quad GSML Deserializer – MAX9286
- FAKRA connectors, supporting:
  - low cost 50Ω Coax (100Ω STP) cables

### 2.2 Block Diagram

The following block diagram provides an overview of the major interfaces (all control signals omitted for clarify).

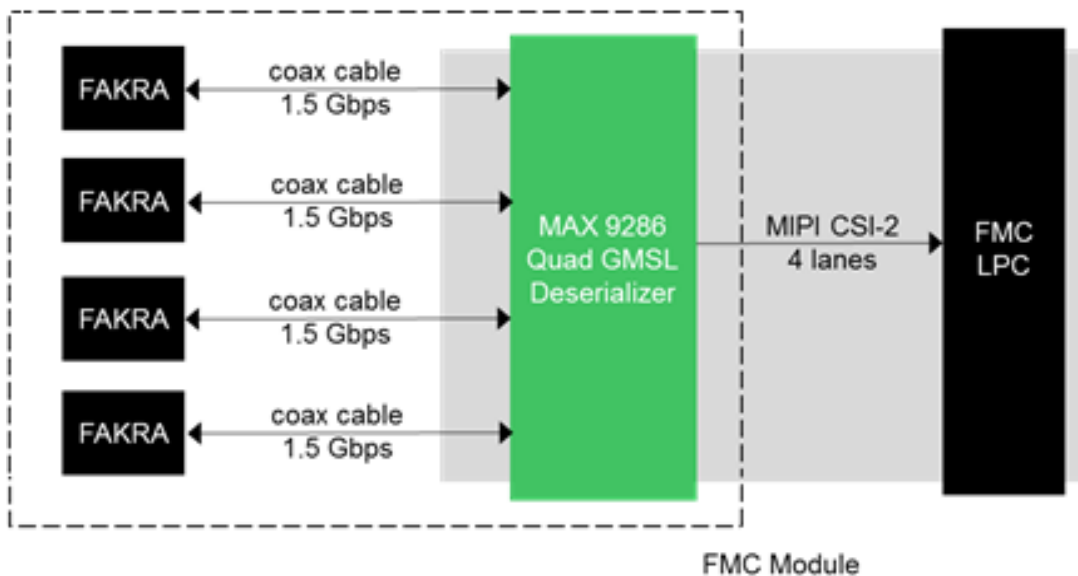


Figure 2 - Avnet Embedded Vision Multi Sensor FMC – Block Diagram

### 3. Functional Description

The following sections provide brief description of each feature provided on the Avnet Embedded Vision Multi-Sensor FMC module.

#### 3.1 FMC LPC

The FMC LPC connector provides 68 single-ended I/O or 34 differential I/O as defined in the following table.

	H	G	D	C
1	VREF_A M2C	GND	PG_C2M	GND
2	PRSNT M2C L	CLK1 M2C P	GND	DP0_C2M P
3	GND	CLK1 M2C N	GND	DP0_C2M N
4	CLK0 M2C P	GND	GBTCLK0 M2C P	GND
5	CLK0 M2C N	GND	GBTCLK0 M2C N	GND
6	GND	LA00 P CC	GND	DP0 M2C P
7	LA02 P	LA00 N CC	GND	DP0 M2C N
8	LA02 N	GND	LA01 P CC	GND
9	GND	LA03 P	LA01 N CC	GND
10	LA04 P	LA03 N	GND	LA06 P
11	LA04 N	GND	LA05 P	LA06 N
12	GND	LA08 P	LA05 N	GND
13	LA07 P	LA08 N	GND	GND
14	LA07 N	GND	LA09 P	LA10 P
15	GND	LA12 P	LA09 N	LA10 N
16	LA11 P	LA12 N	GND	GND
17	LA11 N	GND	LA13 P	GND
18	GND	LA16 P	LA13 N	LA14 P
19	LA15 P	LA16 N	GND	LA14 N
20	LA15 N	GND	LA17 P CC	GND
21	GND	LA20 P	LA17 N CC	GND
22	LA19 P	LA20 N	GND	LA18 P CC
23	LA19 N	GND	LA23 P	LA18 N CC
24	GND	LA22 P	LA23 N	GND
25	LA21 P	LA22 N	GND	GND
26	LA21 N	GND	LA26 P	LA27 P
27	GND	LA25 P	LA26 N	LA27 N
28	LA24 P	LA25 N	GND	GND
29	LA24 N	GND	TCK	GND
30	GND	LA29 P	TDI	SCL
31	LA28 P	LA29 N	TDO	SDA
32	LA28 N	GND	3P3VAUX	GND
33	GND	LA31 P	TMS	GND
34	LA30 P	LA31 N	TRST L	GA0
35	LA30 N	GND	GA1	12P0V
36	GND	LA33 P	3P3V	GND
37	LA32 P	LA33 N	GND	12P0V
38	LA32 N	GND	3P3V	GND
39	GND	VADJ	GND	3P3V
40	VADJ	GND	3P3V	GND

Table 1 – FMC LPC Connector Pinout

**Note:** For the FMC LPC, the connector columns K, J, F, E, B, and A are not used and not shown in the above table.

According to MIPI CSI-2 RX Sub-system documentation, the MIPI pin selection must respect the following requirements:

- RX CLK must be assigned to DBC / QBC / GC\_QGC.
- Continuous IO pair to be used without leaving IO pairs.

Excerpt from documentation:

The MIPI CSI-2 RX Subsystem provides an I/O planner feature for I/O selection. In the Pin Assignment tab, dedicated byte clocks (DBC) or quad byte clocks (QBC) are listed for the clock lane for the selected HP I/O bank. For the QBC clock lane, all of the I/O pins are listed for data lane I/O selection but for the DBC clock lane only the byte group I/O pins are listed for data lane I/O selection.

Eight MIPI CSI-2 RX Subsystem IP cores can be implemented per IO bank based on BITSlice and BITSlice\_CONTROL instances in the UltraScale+ devices.

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**IMPORTANT:** If the RX data lane I/O pins are selected non-contiguously then an additional one, two, or three I/O pins (RX\_BITSLICE) are automatically used for clock/Strobe propagation. Therefore, **it is recommended that you select adjacent I/O pins for the RX configuration to make efficient use of the I/O.** The propagation of strobes to the RX data pins follows the inter-byte and inter-nibble clocking rules given in the UltraScale Architecture SelectIO Resources User Guide (UG571).

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According to the previously mentioned requirements, the following MIPI pin assignments have been found:

MIPI CSI-2 RX Interface	Signal	ZCU104 pin mapping (FMC LPC)	ZCU102 pin mapping (FMC HPC0)	ZCU102 pin mapping (FMC HPC1)	UZEV pin mapping (FMC HPC)
1 Quad-GSML (MAX9686)	CLK	LA00 F17,F16	LA00 Y4,Y3	LA00 G6,G7	LA00 AF16,AF17
	D0	LA01 H18,H17	LA01 AB4,AC4	LA01 AJ6,AJ5	LA01 AD17,AE17
	D1	LA09 H16,G16	LA09 W2,W1	LA09 AE2,AE1	LA09 AK17, AK18
	D2	LA12 G18,F18	LA12 W7,W6	LA12 AD7,AD6	LA12 AJ14,AK14
	D3	LA13 G15,F15	LA13 AB8,AC8	LA13 AG8,AH8	LA13 AJ15,AK15
	<i>strobe prop.</i>	-	LA06 AC2,AC3 LA14 AC7,AC6	LA06 AH2,AJ2 LA14 AH7,AH6	LA10 AG16,AH16 LA16 AG13, AH13

**Table 2 – MIPI CSI-2 RX pin mapping**

The FMC pin allocation for the FMC-MULTICAM FMC Module is defined in the following table.

	H	G		D	C	
1	-	GND	1	PG_C2M	GND	1
2	PRSNT_M2C_L		2	GND	-	2
3	GND		3	GND	-	3
4		GND	4	-	GND	4
5		GND	5	-	GND	5
6	GND	MAX9286_CLK_P	6	GND	-	6
7	I2C_MUX_SCL	MAX9286_CLK_N	7	GND	-	7
8	I2C_MUX_SDA	GND	8	MAX9286_D0_P	GND	8
9	GND	I2C_MUX_RST_N	9	MAX9286_D0_N	GND	9
10	MAX9286_PWDN_N	MAX9286_FSYNC	10	GND	<i>strobe propagation</i>	10
11	POC1_INT_N	GND	11		<i>strobe propagation</i>	11
12	GND		12		GND	12
13	POC1_EN		13	GND	GND	13
14	POC2_INT_N	GND	14	MAX9286_D1_P	<i>strobe propagation</i>	14
15	GND	MAX9286_D2_P	15	MAX9286_D1_N	<i>strobe propagation</i>	15
16	POC2_EN	MAX9286_D2_N	16	GND	GND	16
17	GMSL2_PWDN_N	GND	17	MAX9286_D3_P	GND	17
18	GND	<i>strobe propagation</i>	18	MAX9286_D3_N	<i>strobe propagation</i>	18
19		<i>strobe propagation</i>	19	GND	<i>strobe propagation</i>	19
20		GND	20		GND	20
21	GND	<i>strobe propagation</i>	21		GND	21
22		<i>strobe propagation</i>	22	GND		22
23		GND	23			23
24	GND		24		GND	24
25	<i>strobe propagation</i>		25	GND	GND	25
26	<i>strobe propagation</i>	GND	26	<i>strobe propagation</i>		26
27	GND		27	<i>strobe propagation</i>		27
28			28	GND	GND	28
29		GND	29	-	GND	29
30	GND		30	TDI	SCL	30
31	<i>strobe propagation</i>		31	TDO <sup>1</sup>	SDA	31
32	<i>strobe propagation</i>	GND	32	3P3VAUX	GND	32
33	GND		33	-	GND	33
34			34	-	GA0	34
35		GND	35	GA1	12POV	35
36	GND		36	3P3V	GND	36
37			37	GND	12POV	37
38		GND	38	3P3V	GND	38
39	GND	VADJ	39	GND	3P3V	39
40	VADJ	GND	40	3P3V	GND	40

**Table 3 – FMC-MULTICAM - LPC Pinout**

<sup>1</sup> TDO is connected to TDI in order not to break the JTAG chain

Description	Single-ended	Differential	Global Clock	Total
<b>I2C Peripheral Configuration</b>				
	3	0	0	3
<b>Quad GMSL Deserializer</b>				
	2	16	2	20
<b>Power over Coax</b>				
	4	0	0	4
<b>TOTAL FMC I/O Requirements</b>				
	9	16	2	27

**Table 4 – FMC I/O Requirements**

## 3.2 Power

The following table lists all the voltage sources available on the FMC-MULTICAM module.

Voltage Name	Voltage	Current	Description
supplied by <b>FMC connector</b>			
3V3AUX	3.3 V		Used by IPMI Identification prior to module power-up.
3V3	3.3 V		Used by Quad GMSL Deserializer (MAX9286) and Power-Over-Cable (MAX20087) devices.
VADJ	1.2V		VADJ = 1.2V required for use of MIPI I/O standards on UltraScale+/ZynqUltraScale+ carriers.
12V	12.0 V		Used by MAX20087 (PoC) devices.
supplied by the FMC-MULTICAM <b>FMC module</b>			
VDD18	1.8V		Used by GMSL (MAX9286) for DVDD, MVDD, MAVDD, VDDIO.

**Table 5 –Voltage Sources**

The following table describes the voltage requirements of the GMSL and GMSL2 circuits.

Voltage	GMSL1 (MAX9286) **		Total requirement
Typ	Power Rails	Max Current (mA)	Current (mA)
1.8V	AVDD+DVDD+MAVDD	430	430
3.3V	IOVDD	1	1

**Table 6 – Power Requirements**

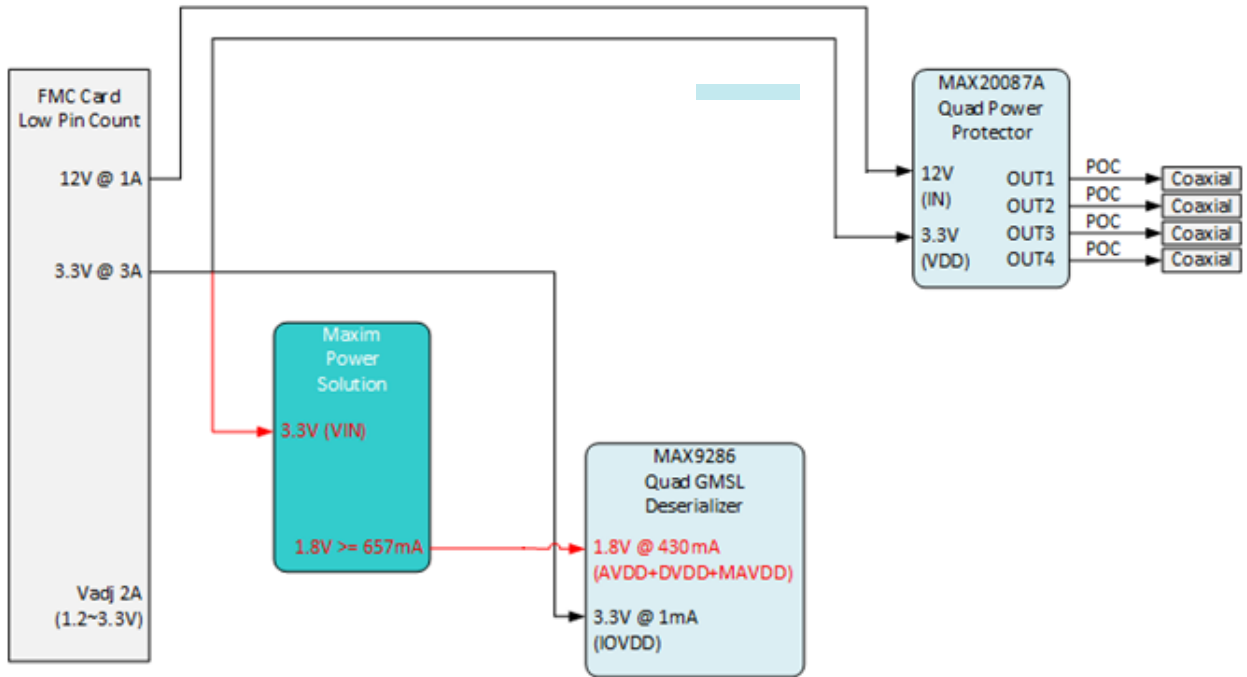
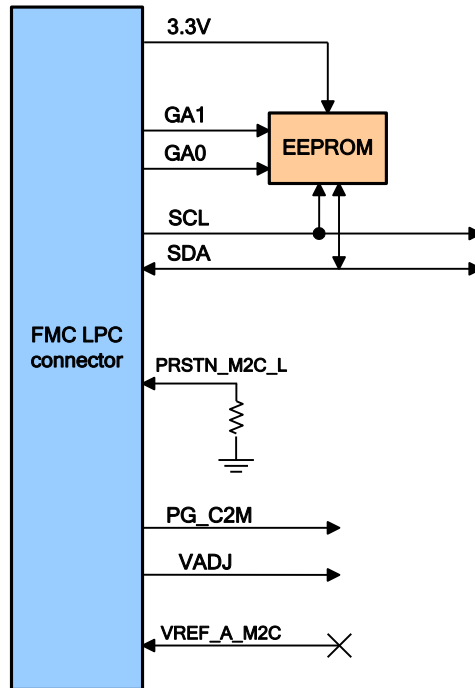


Table 7 – Power, Block Diagram

### 3.3 I2C Chain 1 - IPMI Identification

The following I2C section implements the IPMI identification for the FMC module.



**Figure 3 – IPMI Identification, Block Diagram**

When the VADJ voltage is valid, the PG\_C2M (ie. power good) will be asserted high. An inverted version of this signal is used to enable all the voltage level translators connected to VADJ.

The address of the I2C EEPROM will be determined by the GA[0:1] signals driven by the carrier.

Table 8 describes the EEPROM address for the FMC module.

GA[0:1]	FMC-MULTICAM I2C EEPROM Address
00	0xA0
01	0xA2
10	0xA4
11	0xA6

**Table 8 – IPMI Identification, I2C EEPROM Address**

The EEPROM content is defined by the Platform Management FRU Information Storage Definition V1.0.

<https://www.intel.com/content/www/us/en/servers/ipmi/information-storage-definition.html>

The EEPROM content can be generated with the following on-line utility:

<https://www.opalkelly.com/tools/fmceepromgenerator/>

For the FMC-MULTICAM module, the content is described in Table 9.

<b>Content</b>	<b>FMC-MULTICAM</b>
<b>Board Information</b>	
- Manufacturer Date/Time	-
- Manufacturer	Avnet
- Product	FMC-MULTICAM
- Serial	{programmed during factory testing}
- Part Number	AES-FMC-MULTICAM-G
- FRU File ID	-
<b>Product Information</b>	
- Manufacturer	Avnet
- Product	FMC-MULTICAM
- Part/Model Number	AES-FMC-MULTICAM-G
- Version	A.01.00
- Serial	{programmed during factory testing}
- Asset Tag	-
- FRU File ID	-
<b>FMC Multi-Records</b>	
- Module	single-width
- P1 Connector	LPC
- P2 Connector	None
- VADJ Voltage	1.2V
- VADJ load limits (mA)	min=10, max=1000
- 3.3V load limits (mA)	min=10, max=1000
- 12V load limits (mA)	min=0, max=0
- Clock direction	Mezzanine to Connector
- Max TCK Rate	10
- P1 Bank A Signals	21
- P1 Bank B Signals	0
- P2 Bank A Signals	-
- P2 Bank B Signals	-
- P1 Transceivers	-
- P2 Transceivers	-

**Table 9 – IPMI Identification, EEPROM Content**

### 3.4 I2C Chain 2 – Peripheral Configuration

The FMC-MULTICAM Module implements two I2C chains. The second I2C chain is used to configure the FMC-MULTICAM module's peripherals.

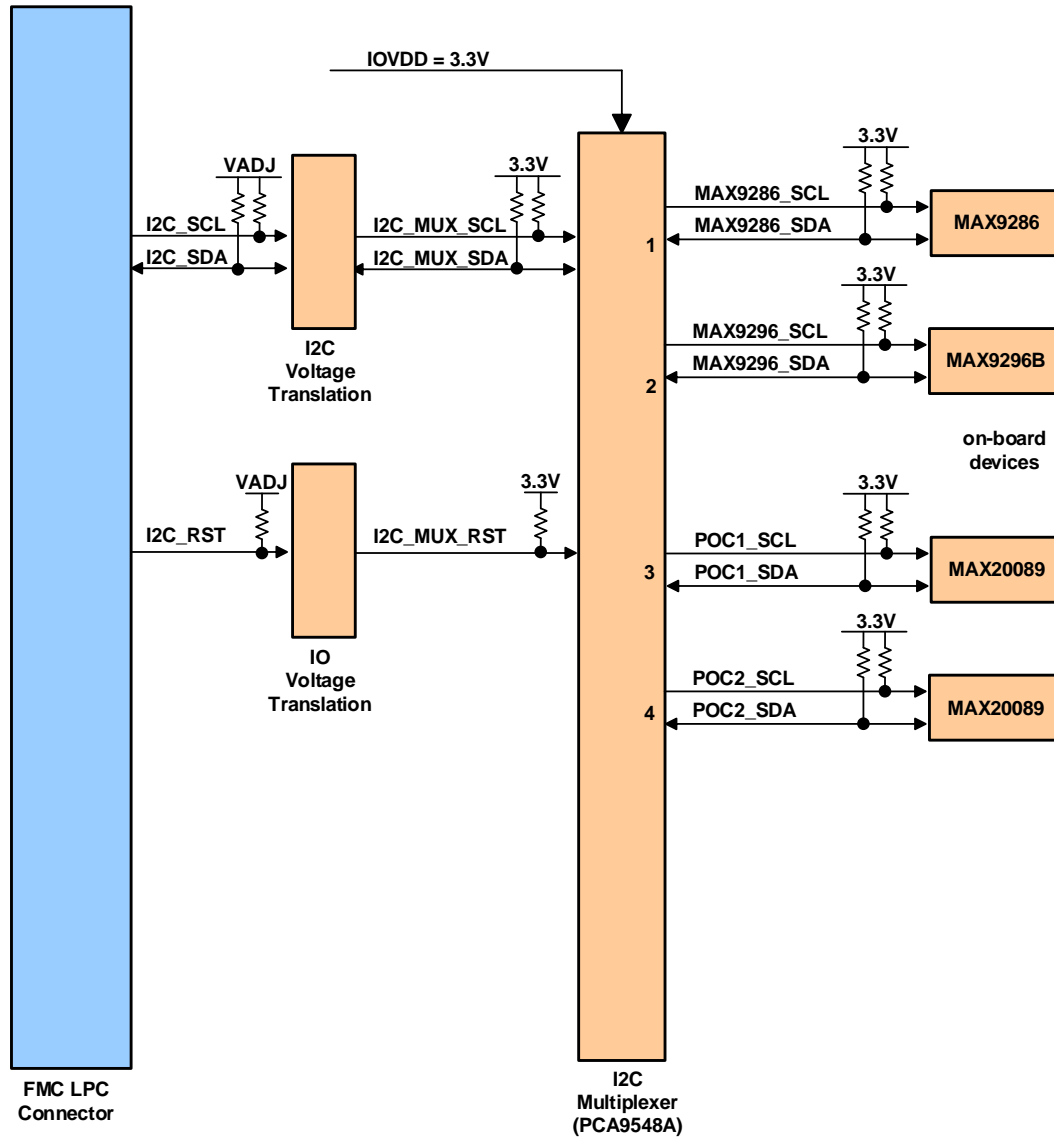


Figure 4 – I2C Peripheral Configuration, Block Diagram

The PCA9546A I2C Multiplexer provides:

- Isolation of each peripheral's I2C chain
- I2C address conflict resolution

The following table lists the I2C addresses that may be present on each of the I2C Multiplexer's ports. Notice that the I2C Multiplexer's address is always visible regardless of which port is enabled.

<b>Device</b>	<b>I2C Address</b>
I2C Multiplexer	0xE0 (PCA9548)
Mux Port 1	
Quad GMSL Deserializer + serializers (4) + image sensors (4)	0x90 (MAX9286)
Mux Port 2	
Unused	
Mux Port 3	
Power Over Coax 1	0x28 (MAX20087A)
Mux Port 4	
Power Over Coax 2	0x28 (MAX20087A)
Mux Port 5	
Unused	
Mux Port 6	
Unused	
Mux Port 7	
Unused	
Mux Port 8	
Unused	

**Table 10 – I2C Peripheral Configuration, Device Summary**

<b>Description</b>	<b>Single-ended</b>	<b>Differential</b>	<b>Global Clock</b>	<b>Total</b>
<b>I2C Peripheral Configuration</b>				
MUX_SCL, MUX_SDA, MUX_RST	3	0	0	<b>3</b>

**Table 11 – Configuration – FMC I/O Requirements**

### 3.5 Quad GMSL Deserializer

The FMC module support up to four (4) 2Mpixel cameras, connected via low cost 50Ω Coax (100Ω STP) cables. The camera modules make use of the Maxim Integrated GMSL (Gigabit Multimedia Serial Link), which includes the following features and advantages:

- compression-free alternative to Ethernet
  - 10x faster data rates
  - 50% lower cabling costs
  - better EMC
- up to 15 meters of 50Ω coax cabling
- built-in spread-spectrum capability, improving EMI performance of the link

The following figure illustrates the MAX9286 based Quad GMSL Deserializer circuit.

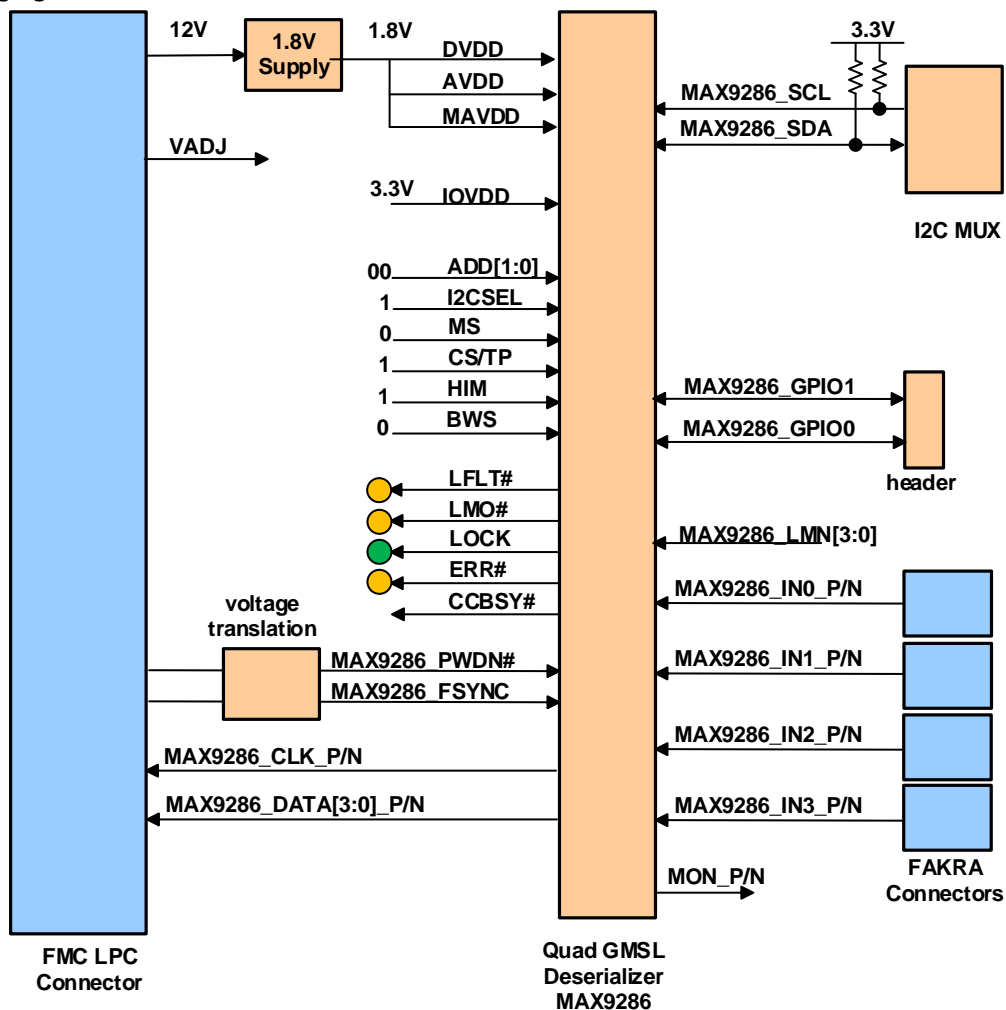


Figure 5 – Quad GMSL Deserializer – Block Diagram

The following table describes the connection of various configuration pins

Pin	Description	Value
ADD[1:0]	Three-Level Address-Selection Input. The state of ADD[1:0] latches at power-up or when resuming from power-down mode (PWDN = low). <b>00 = 0x90</b>	00
I2CSEL	I2C Select. Control-channel interface protocol select input with internal pulldown to EP. <b>Set I2CSEL = high to select I2C-to-I2C interface.</b> Set I2CSEL = low to select UART/UART or UART/I2C interface.	1
MS	Mode Select Input with Internal Pulldown to EP. Mode selection is only used in UART-to-UART and UART-to-I2C mode. Set MS = low to select base mode. Set MS = high to select bypass mode.	0
CX/TP	Coax/Twisted-Pair Select Input with Internal Pulldown to EP. <b>Set CX/TP high to select coax input.</b> Set CX/TP low for STP input. Input cable type can be programmed to a different value after power-up	1
HIM	High-Immunity Mode Input with Internal Pulldown to EP. Default HIGHIMM bit value is latched at power-up or when resuming from power-down mode (PWDN = low) and is active-high. HIGHIMM can be programmed to a different value after power-up. HIGHIMM in the serializer must be set to the same value. High-immunity mode must be supported by the serializer (MAX9275-MAX9281 only).	1
BWS	Three-Level Bus-Width Select Input. Set BWS to the same level on both sides of the serial link. <b>Set BWS = low for 24-bit mode.</b> Set BWS = high for 32-bit mode. Set BWS = open for high-bandwidth mode (MAX9275-MAX9281 only).	0

**Table 12 – Quad GMSL Deserializer – Configuration Pins**

The following table describes the connection of various status pins.

Pin	Description	Connection
LFLT#	Active-Low Open-Drain Line-Fault Output. LFLT has a 60kΩ pullup to IOVDD. LFLT = low indicates a line fault. LFLT is output high when PWDN is low.	YELLOW LED
LMO#	Line Memory-Overflow Output. LMO has a 60kΩ pullup to IOVDD. LMO = low when the serial data overflows the line memory.	YELLOW LED
LOCK	Open-Drain Lock Output with Internal 60kΩ Pullup to IOVDD. LOCK = high indicates that PLLs are locked with correct serial-word-boundary alignment.	GREEN LED

	LOCK = low indicates that PLLs are not locked or an incorrect serial-word-boundary alignment. LOCK is high when PWDN = low.	
ERR#	Active-Low Error Output. Open-drain data error detection and/or correction indication output with internal 60kΩ pullup to IOVDD. ERR is high when PWDN is low.	YELLOW LED
CCBSY#	Active-Low Control-Channel Busy Output. Open-drain indicator of control-channel activity with Internal 60kΩ pullup to IOVDD. CCBSY = low indicates that the control channel is currently in use.	Test Point

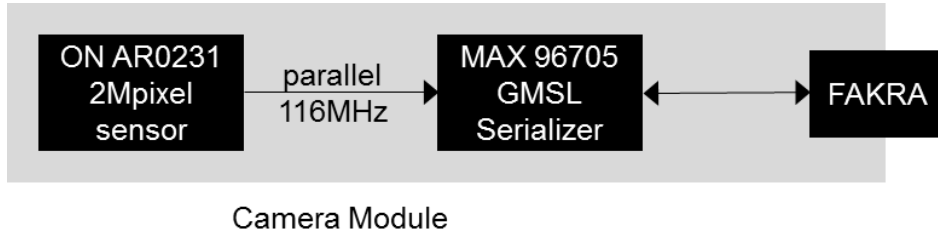
**Table 13 – Quad GMSL Deserializer – Status Pins**

Description	Single-ended	Differential	Global Clock	Total
<b>Quad GMSL Deserializer</b>				
MIPI-CSI2 4 lanes (CLK_P/N, DATA[3:0]_P/N)		8	2	<b>10</b>
Control signals (PDWN#, FSYNC)	2			<b>2</b>
Unuseable (strobe propagation)		8		<b>8</b>
<b>TOTAL</b>	<b>2</b>	<b>16</b>	<b>2</b>	<b>20</b>

**Table 14 – Quad GMSL Deserializer – FMC I/O Requirements**

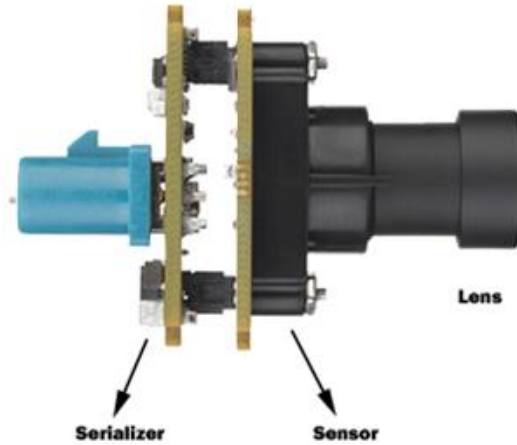
### 3.6 2Mpixel Camera Module

The following figures illustrates the supported 2Mpixel Camera Module



**Figure 6 – 2Mpixel Camera Module – Block Diagram**

The 2Mpixel Camera module is composed of existing off-the-shelf components from ON Semiconductor’s Modular Automotive Reference System (MARS).



**Figure 7 – 2Mpixel Camera Module – MARS Components**

The following table lists the part numbers that make up the supported 2Mpixel camera module.

Part Number	Hardware
2Mpixel Camera Modules	
MARS1-AR0231AT6-GEVB	On Semi MARS AR0231 camera board
MARS1-MAX96705-GEVB	ON Semi MARS MAX96705 Serializer board

**Table 15 – 2Mpixel Camera Module - Components**

### 3.7 Power Over Coax

In order to power the various cameras, the MAXIM Integrated MAX20087A delivers up to 600mA load current to each of its four output channels.

The following figure illustrates the Power Over Coax circuits.

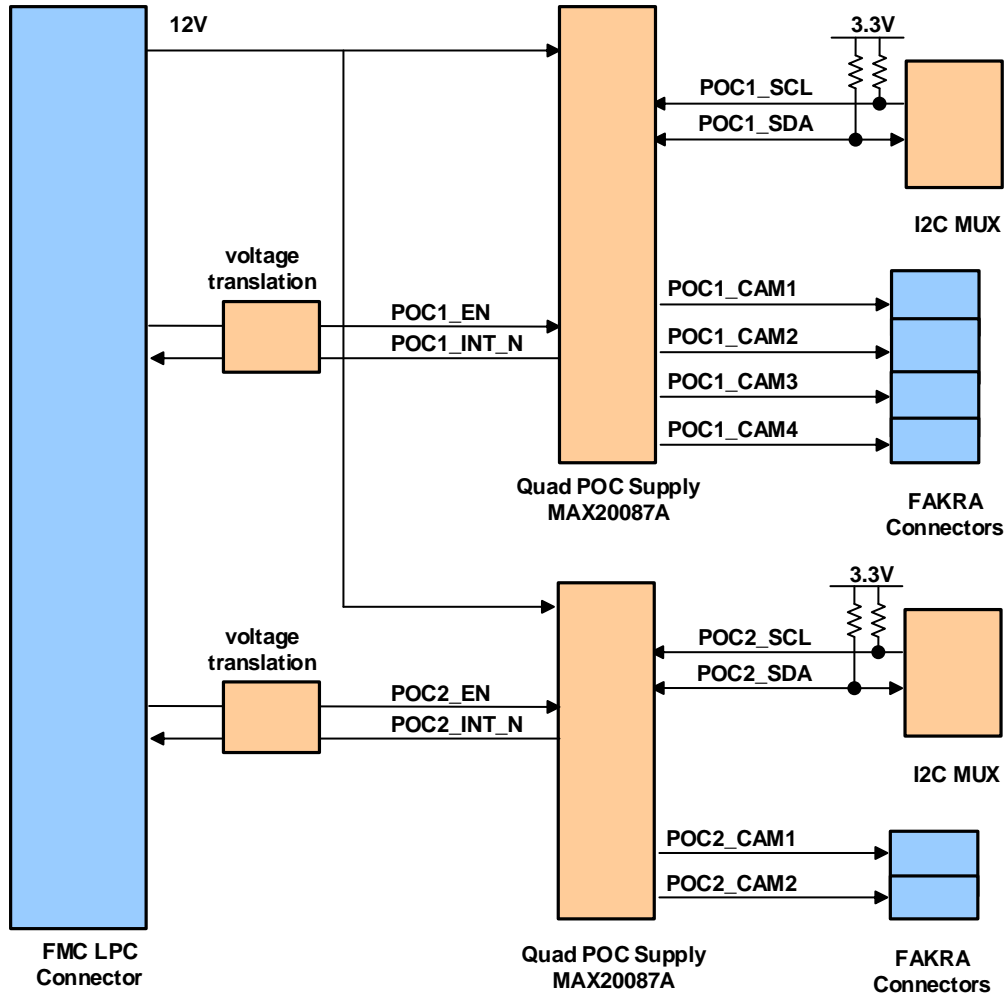


Figure 8 – Power Over Coax – Block Diagram

For the 2Mpixel camera modules, the required power per camera is:

- MAX96705 Serializer = 1.8V @ 128mA
- AR0234 Image Sensor < 350mW

Description	Single-ended	Differential	Global Clock	Total
<b>Dual GMSL2 Deserializer</b>				
Control signals (EN, INT_N)	4			4
<b>TOTAL</b>	<b>4</b>	<b>0</b>	<b>0</b>	<b>4</b>

Table 16 – Power over Coax – FMC I/O Requirements

### 3.8 FAKRA Connectors and Coax Cables

The FMC module makes use of the Rosenberger High-Speed FAKRA Mini (HFM) connectors.

[www.rosenberger.com/hfm](http://www.rosenberger.com/hfm)



The HFM PCB Quad Plug connector used for GMSL is

- Rosenberger : **AMS22D-40MZ5-Z**



The Quad HFM to 4 x FAKRA cable assembly used for the quad GMSL cameras is:

- Rosenberger : **L02-027-1000-Z-ZZZZ\_V2**

